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**TRANSMITTAL LETTER**  
**(General - Patent Issued)**

Docket No.  
EN9-99-008 US2

Patent No. (a) 7,037,753  
Inventor(s) Rodsky et al.

U.S. Patent No.

7,037,753

Issue Date

05/02/2006

Title: **NON-PLANAR SURFACE FOR SEMICONDUCTOR CHIPS**

COMMISSIONER FOR PATENTS:

Transmitted herewith is:

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No fee required below. Errors were made by the United States Patent Office.

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*Jack P. Friedman*  
Signature

Dated: May 22, 2006

Jack P. Friedman, Ph.D.  
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I certify that this document and fee is being deposited on May 22, 2006 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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# UNITED STATES PATENT AND TRADEMARK OFFICE

## CERTIFICATE OF CORRECTION

PATENT NO : 7,037,753

DATED : May 2, 2006

INVENTOR(S) : Brodsky et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page

Under Foreign Patent Documents, add:

-- 5-36825 1993 Japan  
4-317355 1992 Japan  
4-253359 1992 Japan  
3-241856 1991 Japan  
2-155231 1990 Japan  
0840332 A2 05/1998 EPO  
2174539 A 11/1986 Great Britain  
EP97118837 02/2000 European Search --

MAILING ADDRESS OF SENDER: Jack P. Friedman, Ph.D.

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PATENT NO. 7/037,753

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